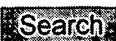




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Device: 0001h LSI53C810 PCI to SCSI I/O **Processor Class:** 01h ... X]
I/O Access: [X] Bus **Master:** [X] Device ...
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The Echelon Lighting Control System

... Others add a **coprocessor** – such as the 8X305 or TMS320 ... The Executive **Processor**
uses multitasking ... A second task is the P4 bus **master**, controlling all transfers ...
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... & hierarchical architecture to **master** complexity and ... bus ... DSP RAM **processor** bus
Communication ... abstract interface to communication **coprocessor**/controller API ...
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EP patents matching keyword 'bus'

... EP347929, Parallel processor. EP426184, Bus **master** command protocol. ... EP267613,
Micro **processor** capable of being connected with **coprocessor**. ...
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Amiga Nostalgia

... Flow, New Horizons, Ideas **Processor**, \$99.95. ... Interactive Movie" game developed by
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... processors where the Arbiter performs classic **DMA** functionality. ... Since the TCU is a
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TechiWarehouse - A+ Questions and Answers

... A: **Master**. 19: What factor determines the amount of RAM a CPU can control? ... 258:
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... Combining the **coprocessor** and general arithmetic instructions yields ... allows the GPP
to be the system **master**. ... modem and a dedicated applications **processor** on a ...
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Astra SysInfo tool v4.10

... crystal (except NexGen Nx586/686); **coprocessor** is identified ... The number is 1 for

single **processor** systems without ... Access, I/O Access, Bus **Master**: Possible ways ...
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ROM BIOS and the first MEG of memory

... 001C, 4, Interrupt Vector for INT 07h (**processor** extension not ... Vector for INT 75h
(IRQ13 math **coprocessor** exception). ... 046C, 4, **master** clock count (long integer) 0 ...
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